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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,451	06/30/2003	Alexander G. MacInnis	14447US01	1633
23446	7590	02/22/2010	EXAMINER	
MCANDREWS HELD & MALLEY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			YENKE, BRIAN P	
ART UNIT	PAPER NUMBER			
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/611,451	Applicant(s) MACINNIS ET AL.
	Examiner BRIAN P. YENKE	Art Unit 2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on *Amendment (12/29/09)*.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 16-27 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 16-27 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Response to Arguments

(from 07/29/09 Non-Final Rejection, which is still pertinent to the present arguments.)

Applicant's arguments with respect to the claims have been considered but are not persuasive.

It is noted the applicant is arguing that it is not obvious to combine the deinterlacer into the video decoder. Initially the examiner notes, these are two different processes/procedures, wherein decoding must be performed prior to deinterlacing, thus the inclusion of the deinterlacing with the decoder, does not negate/change the steps/functions of either procedure, this is supported by the rejection below.

The rejection is made below based upon the concept as disclosed by the below references, that functions may be combined/integrated or not, this is known in the field of endeavor.

Applicant's Arguments

- a) Applicant repeats the previous argument that nowhere in Wells is there any disclosure of the deinterlacing occurring within the decoder.
- b) Applicant states that Wells discloses in one embodiment that scaling is performed after temporal filtering and deinterlacing in the single post-processing stage as opposed to within the decoder.
- c) Applicant states that Wells sets forth an alternative embodiment for adding the deblocker to the decoder but not disclosing alternative embodiments for adding the (MC) temporal filter and/or the (MC) deinterlacer to the decoder.
- d) Regarding Choi applicant states fails to remedy the deficiencies of Wells since Choi teaches integrating components, wherein the claim recites the decoder and display engine (scalar) are separate components.

Examiner's Response

a) The examiner disagrees. Wells explicitly recites an integrated video decoder which includes a video decoder and an integrating post-processing stage. Thus as stated previously the integration/separation of parts is a known practice, whether to put all components on a single chip or multiple chips. The distinction pertains to the arrangement and not the executed function. The signal still must first be decoded, then deinterlaced.....whether integrated or not. The examiner also notes that scaling can be done prior to deinterlacing (as applicant suggest is done in the prior art), however in addition scaling may also be done simultaneously (see cited 20060238650) or after as done by Wells, and cited (20020101535).

b) As stated above in a), the function of scaling or deinterlacing is not changed whether a function is located inside the same circuit block or not. In the event the applicant disagrees the examiner requests applicant to clarify such.

c) The examiner notes as stated above, the integrated decoder of Wells includes and integrated post-processing stage. Although Wells discloses an embodiment that the deblocker may be added to the decoder, this emphasizes the examiner's position that the functions can hardwired/connect in a number of ways, whether integrated or separate, either way the respective functions are independently carried out, decoding must occur before deinterlacing, and scaling can occur prior/simultaneously or after deinterlacing as known in the art.

d) The examiner agrees that Choi integrates components. Choi was incorporated to show that all processing functions can be included on a single chip, as opposed to prior art wherein the elements were separated. Thus Choi was included to evidence that it is known to incorporate elements on a single chip or have the functions separate, wherein the functions still perform their intended function.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wells, US 2004/0057624 in view of Choi, US 7,206,025.

In considering claims 16 and 22,

Wells discloses an integrated video decoder 202 (Figs 3-8) which includes the decompression engine, which also includes a deinterlacer and scaler (para 0014, 0016), wherein the scaler is met by post processing stage 206.

Wells discloses in the prior art and in one embodiment (Fig 3) that in a non-integrated system the decoder and deinterlacing chip are on separate chips (para 0014, 0033). The invention of Wells to provide an integrated video decoding system in which in one embodiment is fully integrated (Fig 7).

Based upon applicant's arguments that Wells does not disclose an integrated decoder, deinterlacer the examiner will evidence such.

The concept of including all process/functions onto a single chip (i.e. which meets the video decoder comprising, since any item within a block/chip comprises the other such items...and the decoder and display engine are discrete components) is conventional practice in the art, as evidenced by Choi, US 7,206,025, which discloses a single chip conversion device (Fig 3).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify/utilize in Wells which discloses an integrated decoder system, to allow the system/designer the option of having all functions/components onto a single chip as done conventionally, which provides instant advantages with space savings and efficient utilization of system resources by such integration.

Regarding the separate components/devices, as evidenced by Wells, components may be either integrated or non-integrated, thus the claimed video decoder and display engine may be integrated or non-integrated (i.e. separate elements).

In considering claims 17-18 and 22-23,

Wells discloses the use of MPEG2 (para 003), wherein Wells discloses that the majority of dominant compression schemes (i.e. MPEG-2) are lossy.

In considering claim 19 and 25,

Wells discloses the use of motion compensation (see para 001, 004, 006, 0017, 28, 31).

In Considering claims 20-21 and 26-27,

As stated above (claim 17) Wells discloses that the majority of compressed images are lossy, however the use of lossless decompression/Huffman decoding are notoriously well known in the field of endeavor in order to recover an image with little/no loss, thus the examiner takes "OFFICIAL NOTICE" regarding such.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (571)272-7359. The examiner work schedule is Monday-Thursday, 0730-1830 hrs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David L. Ometz, can be reached at (571)272-7593.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571)-273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)305-HELP.

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800-PTO-9199 or 703-308-HELP

(FAX) 703-305-7786

(TDD) 703-305-7785

An automated message system is available 7 days a week, 24 hours a day providing informational responses to frequently asked questions and the ability to order certain documents. Customer service representatives are available to answer questions, send materials or connect customers with other offices of the USPTO from 8:30 a.m. - 8:00p.m. EST/EDT, Monday-Friday excluding federal holidays.

For other technical patent information needs, the Patent Assistance Center can be reached through customer service representatives at the above numbers, Monday through Friday (except federal holidays) from 8:30 a.m. to 5:00 p.m. EST/EDT.

The Patent Electronic Business Center (EBC) allows USPTO customers to retrieve data, check the status of pending actions, and submit information and applications. The tools currently available in the Patent EBC are Patent Application Information

Retrieval (PAIR) and the Electronic Filing System (EFS).

PAIR (<http://pair.uspto.gov>) provides customers direct secure access to their own patent application status information, as well as to general patent information publicly available. EFS allows customers to electronically file patent application documents securely via the Internet. EFS is a system for submitting new utility patent applications and pre-grant publication submissions in electronic publication-ready form. EFS includes software to help customers prepare submissions in extensible Markup Language (XML) format and to assemble the various parts of the application as an electronic submission package. EFS also allows the submission of Computer Readable Format (CRF) sequence listings for pending biotechnology patent applications, which were filed in paper form.

/BRIAN P. YENKE/
Primary Examiner, Art Unit 2622

B.P.Y.
17 Feb 10

Application/Control Number: 10/611,451
Art Unit: 2622

Page 8